Claims

What is claimed is:

1. An electronic interface for connecting to a network having a data stream placed on a bus high signal and a bus low signal, comprising:

a ground synthesizer circuit, coupled to the bus high signal and bus low signal, configured to synthesize a ground from the bus high signal and bus low signal;

a capacitive isolator circuit, coupled to the ground synthesizer circuit, configured to generate an isolated bus high signal from the bus high signal; and

an edge triggering circuit, coupled to the capacitive isolator circuit, configured to regenerate the data stream into a first reconstructed data stream by comparing the isolated bus high signal with the ground.

2. The electronic interface of claim 1, wherein the ground synthesizer is further operable to utilize a ground input as a ground signal.

3. The electronic interface of claim 1, further comprising an input protection circuit coupled to receive inputs from the bus high signal and bus low signal and for transmitting protected signals to the ground synthesizer circuit.

4. The electronic interface of claim 3, wherein the input protection circuit is further operable to receive a power input and a ground input.

5. The electronic interface of claim 4, wherein the power input and ground input are connected through an impedance to limit the load on the power input.

6. The electronic interface of claim 1, wherein the capacitive isolator further comprises a capacitor and a resistor in series between the bus high signal and the isolated bus high signal.

7. The electronic interface of claim 1, wherein the edge triggering circuit further comprises a differential amplifier coupled with the capacitive isolator circuit to reconstruct the data stream by comparing the isolated bus high signal with the ground.

8. The electronic interface of claim 7, wherein the differential amplifier is also configured as a schmitt trigger for switching of the amplifier.

9. The electronic interface of claim 1, wherein the capacitive isolator circuit is further coupled with a bus low signal and a ground to receive a low data stream and operable to generate an isolated bus low signal from the bus low signal; and

the edge triggering circuit is further operable to regenerate the data stream into a second reconstructed data stream by comparing the isolated bus low signal with the ground.

10. The electronic interface of claim 9, further including:

a combinatorial data circuit coupled with the edge triggering circuit to receive the first reconstructed data stream and the second reconstructed data stream for generating an output bitstream from the first reconstructed data stream and the second reconstructed data stream.

11. The electronic interface of claim 10, wherein the combinatorial data circuit further comprises a differential amplifier coupled with the edge triggering circuit to receive the first reconstructed data stream and the second reconstructed data stream for comparing the first reconstructed data stream with the second reconstructed data stream and generating the output bitstream based on the comparison.

12. The electronic interface of claim 1, further comprising a combinatorial fault circuit coupled to the capacitive isolator circuit to receive a data high pump signal and operable to analyze the first reconstructed data stream and generating a fault if the first reconstructed data stream fails to transition as indicated by the data high pump signal.

13. The electronic interface of claim 12, wherein the combinatorial fault circuit further comprises a data pump coupled to the capacitive isolator circuit for receiving a data high pump signal, the data pump in series with a charging capacitor, the charging capacitor placed in series with a resistor and in parallel with the base of a transistor, such that when the charging capacitor discharges through the resistor the transistor turns off, triggering a fault signal.

14. A method of reconstructing an input data stream into an output data stream, comprising:

capacitively isolating the input data stream to form a data stream of edge pulses;

comparing the data stream of edge pulses to a ground signal; and

latching the output data stream high upon a positive edge pulse and latching the output data stream low upon a negative edge pulse to create the output data stream.

15. The method of claim 14, further comprising:

capacitively isolating a second input data stream to form a second data stream of edge pulses;

comparing the second data stream of edge pulses to the ground signal;

latching a second output data stream high upon a second data stream negative edge pulse and latching the second output data stream low upon a second data stream negative edge pulse; and

comparing the output data stream and the second output data stream to form a third output data stream.

16. The method of claim 15, further comprising:

generating the ground signal from a combination of the first input data stream and the second input data stream; and

capacitively isolating the ground signal from the first input data stream and the second input data stream.

17. The method of claim 15, further comprising:

receiving the ground signal from an input ground signal.

18. The method of claim 17, further comprising:

receiving an input power signal; and

coupling the input power signal to the input ground signal through an impedance to prevent overloading a power source.

19. The method of claim 14, further comprising:

monitoring the output data stream for the presence of an active data stream; and

triggering a fault condition upon the absence of the active data stream.

20. An electronic interface for connecting to a network having a data stream placed on a bus high signal and a bus low signal, comprising:

a synthesizing means coupled to the bus high signal and the bus low signal for synthesizing a ground from the bus high signal and bus low signal;

an isolating means coupled to the synthesizing means for receiving the bus high signal from the synthesizing means and the ground from the synthesizing means and for generating an isolated bus high signal from the bus high signal; and

a reconstruction means coupled to the isolating means for receiving an isolated bus high signal and a ground and for reconstructing the data stream by comparing the isolated bus high signal with the ground.

21. An electronic interface for connecting to a network having a data stream placed on a bus high signal and a bus low signal, comprising:

a ground synthesizer circuit coupled to the bus high signal and the bus low signal and configured to create a synthesized ground from the bus high signal and bus low signal; and

a capacitive isolator circuit coupled to the ground synthesizer circuit and for receiving the bus high signal and the bus low signal and configured to generate an isolated bus high signal from the bus high signal, an isolated bus low signal from the bus low signal, and an isolated ground from the synthesized ground.

22. The electronic interface of claim 21, wherein the ground synthesizer circuit comprises:

a first resistor placed in series between the bus high signal and the synthesized ground; and

a second resistor placed in series between the bus low signal and the synthesized ground.

23. The electronic interface of claim 22, wherein the resistors provide substantially the same resistance.

24. The electronic interface of claim 21, wherein the capacitive isolator circuit comprises:

a first capacitor and a first resistor in series between the isolated bus high signal and the bus high signal;

a second capacitor and a second resistor in series between the isolated bus low signal and the bus low signal; and

a third capacitor and a third resistor in series between the isolated synthesized ground and the synthesized ground.